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Reducing The Number Of Transistors In Carry Select Adder

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Abstract: **In existing method CMOS logic involved in carry select adder (CSLA), the data dependencies and redundant logic operations are analyzed and then reduced. The carry select (CS) operation is arranged before the calculation of-final-sum, which varies from the earlier methods. But the method is not much more efficient due to power consumption is high. This paper shows the comparison of CMOS logic design and modified Gate Diffusion Input logic (Mod-GDI) and proved Mod-GDI logic is more power-efficient than Gate Diffusion Input logic (GDI), Pass Transistor Logic (PTL) and CMOS logic design in CSLA. Basic GDI logic suffers from some limitations like swing degradation, fabrication difficulty in standard CMOS process and bulk connections. These limitations can be overcome by Mod- GDI. In the proposed scheme, Mod-GDI is better than GDI and CMOS in the maximum cases with respect to area, speed, and power dissipation, and power-delay products. From the simulation results, 45% reduction in power-delay product in Mod-GDI logic in CSLA is obtained. Mod-GDI technique performs varies logic functions by using two transistors. Mod-GDI logic is suitable for designing high speed and less power consumption with reduced number of transistors. Finally, we compare the power consumption and time delay of the existing method with our proposed scheme to show our achievement on accuracy.**

Keywords: **Adder, Low power, GDI and Mod-GDI.**

I. INTRODUCTION

Nowadays portable appliances and mobile phones requires low power, delay, area-efficient and high speed VLSI systems [1,2].Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. Several variants of different logic styles have been proposed to implement 1-bit adder cells, in recent years

These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. Designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives in mobile applications.

The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. When an electronic device such as a mobile phone is in standby mode, the phone is in talk mode, are shut down even though certain portions of the circuitry within the electronic device, which are active.

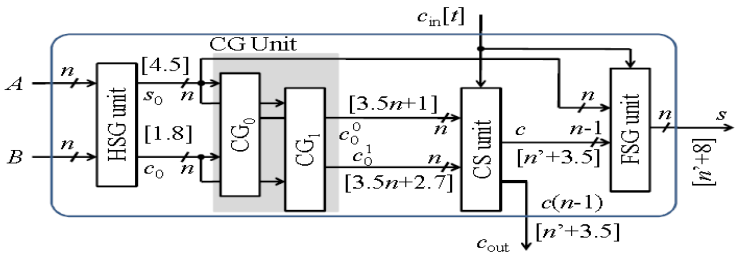
Adder plays an important role in basic arithmetic computation since more complex computation on multiplier and divider circuits.

II. BACK GROUND

A. Existing adder design:

Existing CSLA design is shown in Fig.1(a) has one half-sum generation (HSG) unit, one full-sum generation (FSG) unit, one carry generator (CG) unit and one carry-select (CS) unit. Two carry-generators (CG0 and CG1) corresponding to

input-carry '0' and '1', which are in the CG unit. The two n bit operands (A and B) are given to HSG, and half-sum word s0 and half-carry word c0 of width n-bit each are generated. The half-sum word s0 and half-carry word c0 is obtained from the HSG unit and it is given to both CG0 and CG1 and then two n-bit full-carry words c01 and c11 is produced corresponding to input-carry'0' and '1', respectively [3].The HSG unit logic diagram is shown in Fig.1.(b). The logic circuits of CG0 and CG1 are enhanced to take the benefits of the fixed input carry bits. The CG0 and CG1 logic diagrams are shown in Fig.1.(c) and (d), respectively. The CS unit design is shown in Fig.1(e) which consists of n AND-OR gates. CS unit generates the final-carry word c. The c's most significant bit (MSB) is given to output as cout and (n−1) LSBs are XORed with (n − 1) MSBs of half-sum (s0) in the FSG unit, which is shown in Fig.1(f) and (n − 1) MSBs of final-sum (s) is received. The LSB of s0 is XORed with cin and LSB of s is received [3].



(a)

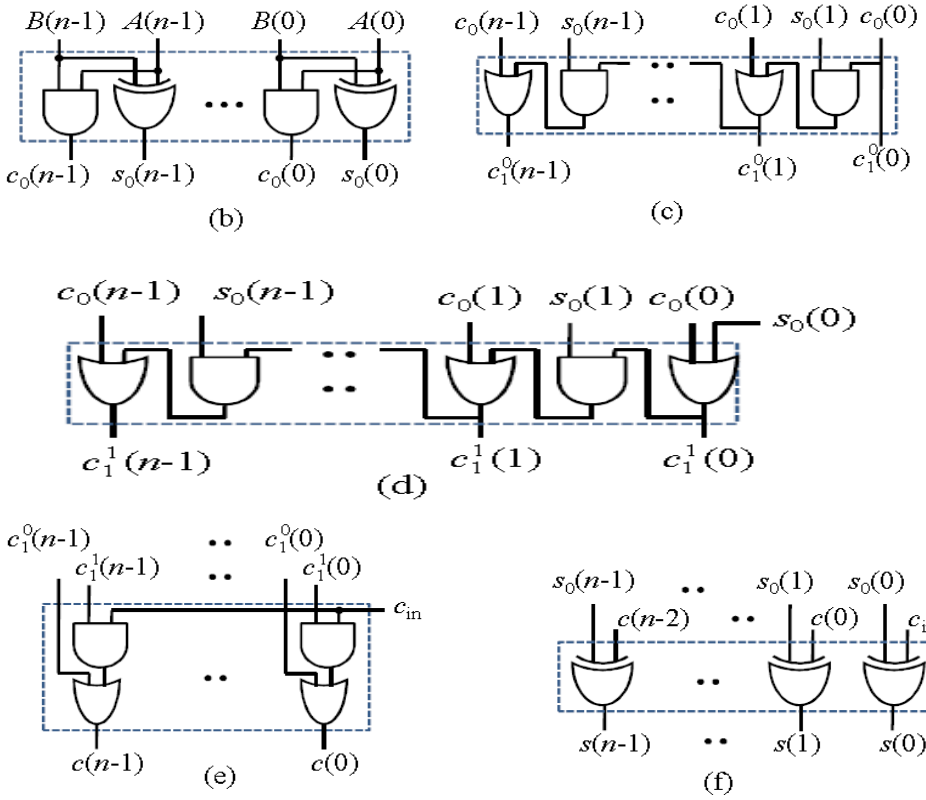


Fig.1(a)Existing carry select adder design, (b) Gate-level design of half sum generator (HSG), (c) Gate-level optimized design of carry-generator (CG0) for input-carry = 0,(d) Gate-level optimized design of carry-generator (CG1) for input-carry=1, (e)Gate-level design of carry-select (CS) unit, (f) Gate-level design of final-sum generation (FSG) unit.

B. Pass transistor logic (PTL):

Many researches on low power, high speed embedded systems such as mobiles, laptops, etc which allows a lot of functions to be integrated on a single chip. The improvement of many logic design techniques during the last two decades, in order to increase the performance of logic circuits, which based on traditional CMOS technology, One form

of logic that is popular in low-power digital circuits is PTL. The earlier method for deriving pass-transistor logic is suitable for NMOS. A set of control signals is given to the gates of NMOS transistors based on the model. N-transistors receives the another set of data signals. The PTL reduces the redundant transistors so it is ulmost common for low power digital circuits[4]. The transistors are functioned as switches in order to pass the logic levels between nodes of a circuit, instead of switches that are directly connected to supply voltages (VDD).

Some of the important advantages of PTL when compared to CMOS design are 1) high speed and low power dissipation due to reduced number of transistors; and 2) Less interconnection effects due to a small area.

PTL has certain disadvantages: 1) Decrease in potential difference between high and low logic levels, at each stage, 2) It's speed reduces when power supply reduces, 3.Static power dissipation is high. GDI is the best method for low power digital circuit design using less number of transistors compared to traditional CMOS design and existing PTL techniques.

C. *GDI technique:*

Power dissipation is the most significant problem in high performance circuits. GDI logic technique which reduces the power consumption, time delay and area of digital circuits, which also reduces the complexity of logic design. Morgenshtein et al. investigated a high-speed and multipurpose logic style for low power [5]-[7].Comparingthearea, number of devices and power dissipation ofCMOS,PTL and GDI design techniques, which shows some advantages and limitations of GDI when compared to other methods. FIG. 2 shows basic GDI logic cell, which is used for implementing logic functions and circuits at low power and high speed design where G, P and N are three inputs and output is taken from D terminal [6]. Table 1 represents the logic functions which can be implemented with the help of this basic GDI cell.

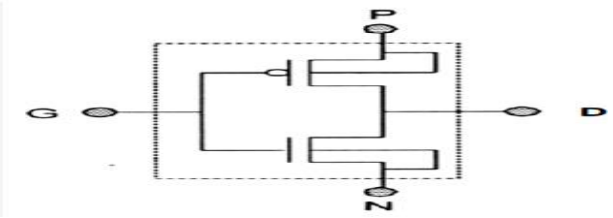


Fig 2: Basic GDI cell

Table 1: Various Logic Functions Implemented with of Basic GDI Cell

N	P	G	D	Functions
Low	B	A	A'B	F1
B	High	A	A' + B	F2
High	B	A	A + B	OR
B	Low	A	AB	AND
C	B	A	A'B + AC	MUX
Low	High	A	A'	NOT

KEY FUNCTIONS OF GDI LOCIC CELL:

The GDI logic style deals with the implementation of a wide range of logic operations and uses only two transistors. GDI logic technique is efficient for design of high-speed and low-power circuits using less number of transistors when compared to CMOS and existing PTL logic techniques. The GDI logic style method uses a simple basic GDI cell, which consists of two transistors with four terminals (3-Input terminal,1-Output terminal).looks closely similar to the basic CMOS inverter at first glimpse and reminds one of the standard CMOS inverter, except present various remarkable differences which are listed below.

1. The basic GDI cell has three inputs such as: G (common gate input of nMOS and pMOS), P (input to source of pMOS), and N (input to source of nMOS) but in CMOS inverter circuit there is no three inputs.

2. The bulk connection of both nMOS and pMOS transistors is made possible with N or P respectively, so it can be arbitrarily biased, which is in contrast with a CMOS inverter.

3. The basic GDI cell allows implementation of varies logic functions using only two transistors which are impossible with CMOS inverter.

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All basic logic gates and universal gates also with this GDI cell; we can conclude that the GDI logic style approach consumes less silicon area compared to other logic styles. GDI gates have lesser area and high speed performance and the logic style is a power efficient method of design.

FUNCTIONAL BLOCK DIAGRAM OF GDI LOGIC CELL:

FIG. 3 shows a simplified functional block diagram of a GDI logic cell, which uses two transistors for the implementation of varies logic functions. Basic GDI logic cell has P logic block, N logic block, first & second logic inputs, and three logic terminals: common diffusion logic terminal and first and second dedicated logic terminals. Depending upon the logic circuit implementation, the first and second dedicated logic terminals and the common diffusion logic terminal which are suitable to perform as a logic signal input terminal or a logic signal output terminal [6,7].

The P logic block has an arrangement of p-type transistors that are interconnected for the purpose of implementation of the logic function. The P logic block contains three logic connections that are as follows; a gate connection is at the gate, an outer diffusion connection at an outer diffusion node, and an inner diffusion connection at the second inner diffusion node of one of the p-type transistors. The first dedicated logic terminal is connected to an outer diffusion connection and the first logic input is given to the gate terminal.

The N logic block has an arrangement of n-type transistors, which is to implement the complementary logic function, and is arranged in similar to that of the P logic block.

Common diffusion logic terminal; the P and N logic blocks has inner diffusion nodes in the common diffusion logic terminal which are connected mutually to form the common diffusion logic terminal.

Common logic input; the common logic input is obtained from the mutual connection of common logic terminals. Therefore, both the P and N logic blocks receive the common logic input.

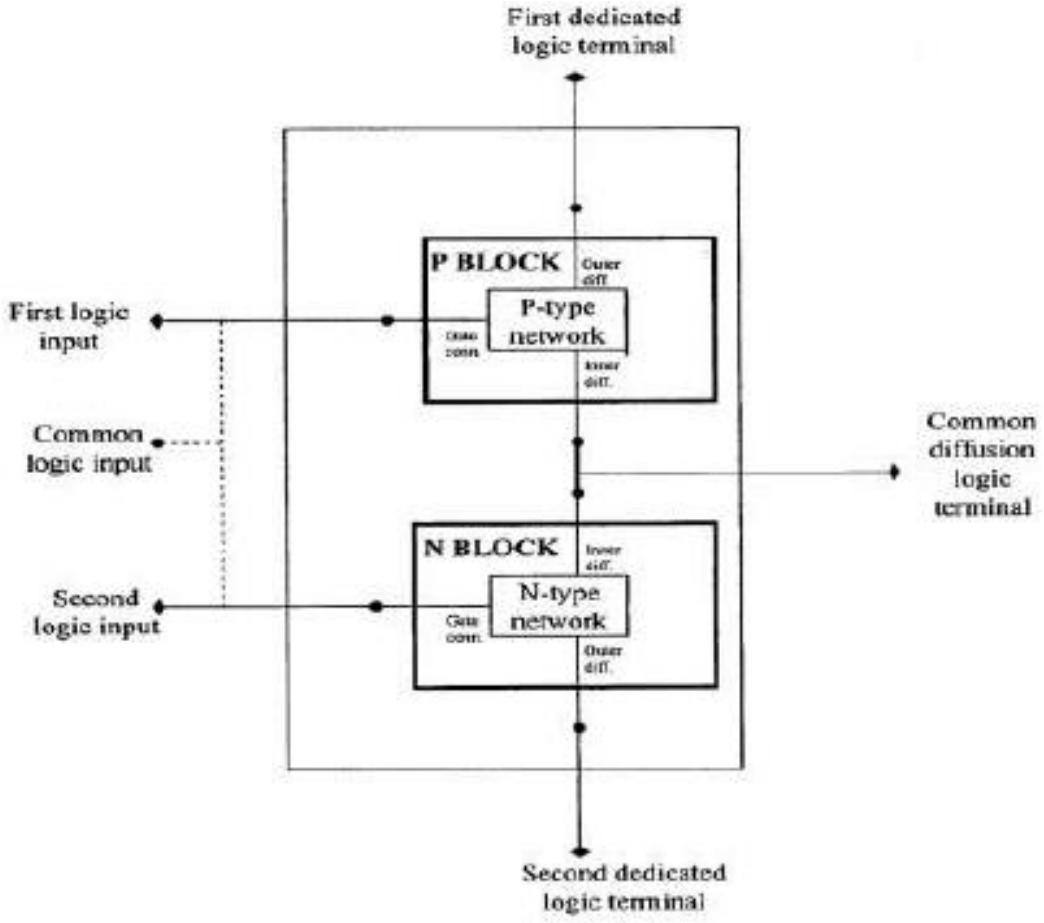

Fig 3: Functional block diagram of a GDI logic cell

GDI CIRCUITS HAVING SOME PRACTICAL LIMITATIONS:

a. GDI circuits also faces problem of swing degradation like PTL circuit design. For eliminating this problem of swing degradation, a method is used for swing restoration in which a buffer stage is used after every GDI cell, presented by Fish et.al [6]. But this is not a good quality solution because adding buffer after every logic cell will lead to increased area and reduced delay.

b. The another most important problem is complexity that GDI logic style faces is difficulty in fabricate in standard CMOS process.

c. The cell area is increased due to the need for separate wells for each transistor, if twin-well process is used for implementation by Fish et.al [7] has proposed a modified version of their GDI cell to make it standard CMOS process compatible.

d. The bulks of nMOS and pMOS are constantly connected to VDD and GND respectively.

The basic GDI logic style has some disadvantages like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by Modified GDI logic style.

III. MODIFIED GDI TECHNIQUE

This technique most popularly deals with reduction of power consumption, area and time delay of digital circuits. Modified-GDI [Mod-GDI] cell has a low-voltage terminal SP and a high-voltage terminal SN, which is designed to connect with a high constant voltage (i.e. supply voltage, VDD) and a low constant voltage (i.e. Ground, GND) respectively, which is in contrast with the basic GDI cell. With the help of these terminals, the Mod-GDI cell is compatible for implementation of all current CMOS technologies. Compared to the existing method, the modified GDI method has less number of transistor and the power consumption and the area is also reduced [5].

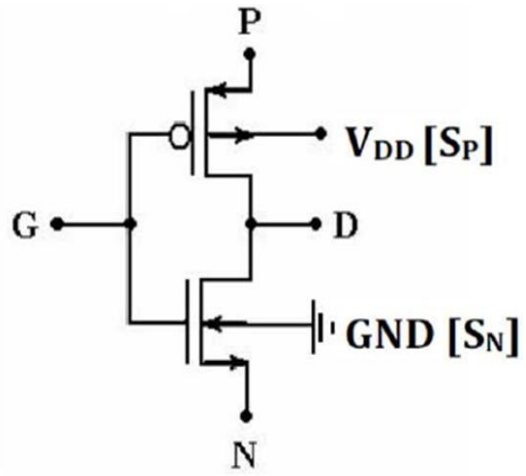

Fig 4: Basic Mod-GDI cell

The bulk connection of PMOS transistor is made with the high constant voltage referred as a supply voltage or VDD and the bulk connection of NMOS transistor is made with the low constant voltage referred as a ground or GND, in the Mod-GDI cell. By doing this, the proposed Mod-GDI cell is completely suitable for implementation in a standard CMOS process of fabrication, since bulk connection of all PMOS transistors are connected to the power supply, VDD and bulk connection of all NMOS transistors are connected to the ground, GND. Mod-GDI technique improves the static power characteristics and logic level swings and also allows simple top-down design methods. The basic Mod-GDI is shown in Fig 4.The four-terminal NMOS and PMOS transistors are used in Mod-GDI cell and can be easily implemented in all type of standard CMOS technology [5].

Table 2 represents the various logic functions which can be implemented with the help of MOD-GDI cell for different input configurations.

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Table 2: Various Logic Functions of Mod-GDI cell for Different Input Configurations

N	S_N	P	S_P	G	D	FUNCTIONS
O	0	1	1	A	A'	INVERTER
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
A'	0	A	1	B	A'B+AB'	XOR
A	0	A'	1	B	AB+A'B'	XNOR
0	0	B	B	A	A'B	FUNCTION 1
B	0	1	1	A	A'+B	FUNCTION 2
C	0	B	1	A	A'B+AC	MUX

This straightforward arrangement as shown in Fig 4 has made the fabrication of GDI cells compatible with the

Standard Nano-scale CMOS fabrication process. Whereas many leakage components can be recognized in sophisticated sub-micron technologies, the most important leakage currents are given below [5]:

1. Sub-Threshold Leakage

2. Gate Leakage (caused by electron tunneling)

This exceptional arrangement of Mod-GDI cell provides considerable reduction of both sub-threshold and gate leakage compared to static CMOS gate.

In order to achieve area efficiency, these methods performs a basis for efficient synthesizer implementation. Such as; Reduction of Short-Circuit Current, Repeaters etc.

Table 3: Comparison of Basic logic gates and CMOS logic design

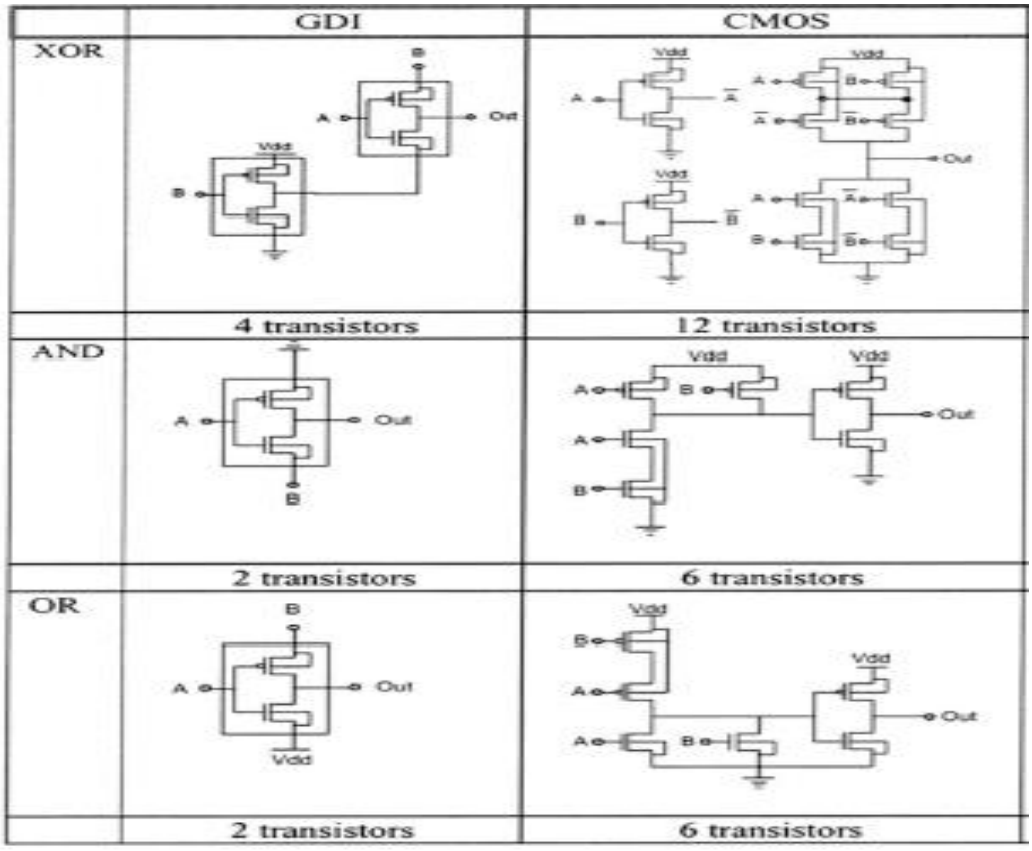

Table 3 shows that GDI logic style as well as Mod-GDI logic style both are superior to CMOS logic style for low power design as the numbers of transistors used for implementing basic logic gates are less than that are used in CMOS logic design.

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IV. SIMULATION RESULT

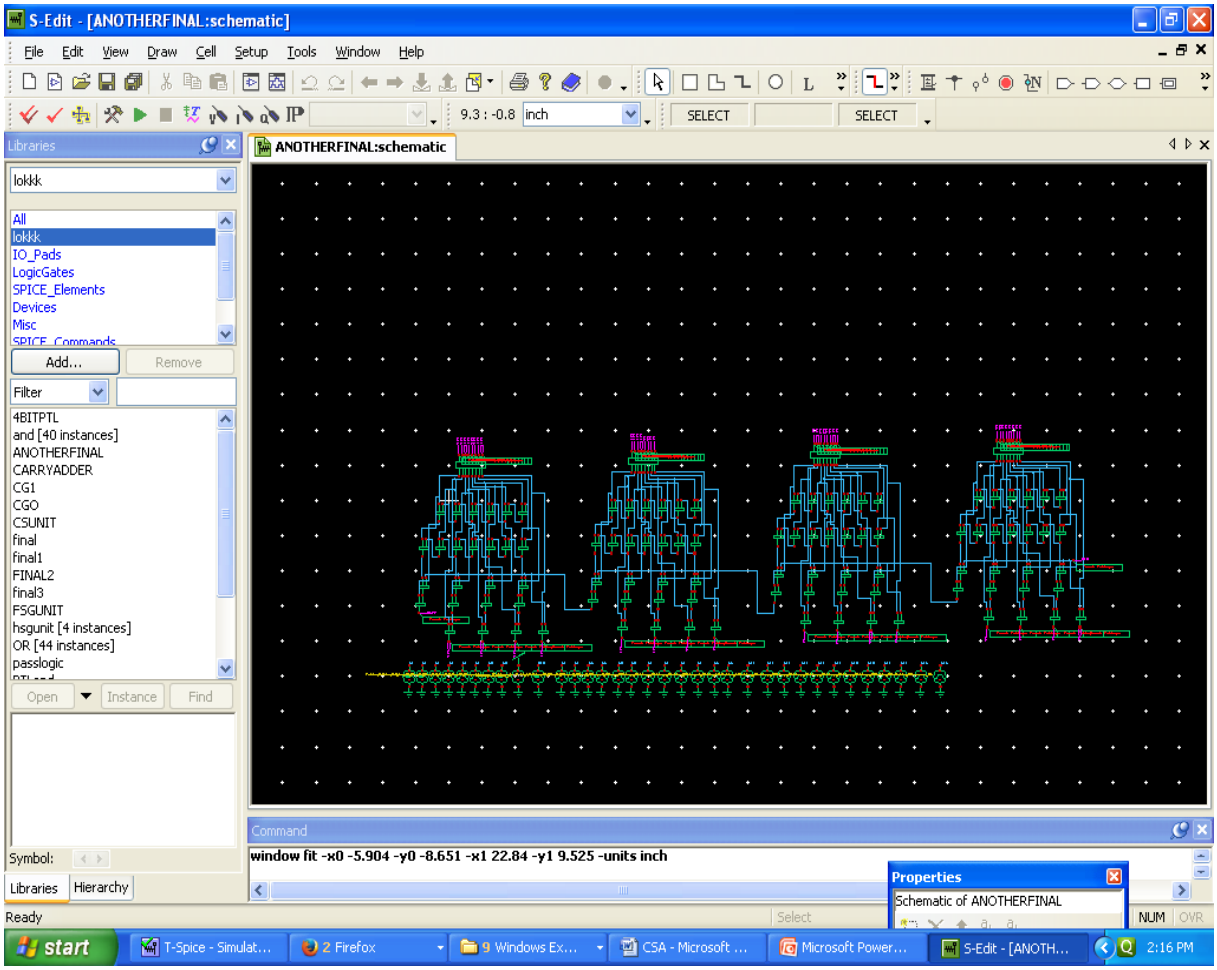

Fig 5: Design for CSLA

Fig 6: Waveform of CSLA

Simulation Results for CMOS logic

```
*  BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 100
Average power consumed -> 4.430748e-011 watts
Max power 7.944081e-001 at time 3.02499e-007
Min power 5.773631e-010 at time 1.13099e-007


*  END NON-GRAPHICAL DATA
*

*  Parsing                                0.01 seconds
*  Setup                                  0.10 seconds
*  DC operating point                     0.19 seconds
*  Transient Analysis                     5.04 seconds
*  Overhead                               1.44 seconds
*  ---------------------------------------------------
*  Total                                  6.78 seconds
```

Simulation Results for MOD-GDI logic

```
*  BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 100
Average power consumed -> 2.694066e-011 watts
Max power 8.352189e-002 at time 4.00535e-007
Min power 1.486583e-008 at time 0

*  END NON-GRAPHICAL DATA
*

*  Parsing                                0.01 seconds
*  Setup                                  0.05 seconds
*  DC operating point                     0.11 seconds
*  Transient Analysis                     1.34 seconds
*  Overhead                               1.08 seconds
*  ---------------------------------------------------
*  Total                                  2.59 seconds
```

Table 4: Comparison of delay & power of logic functions in MOD-GDI and CMOS logic

CMOS LOGIC			MOD-GDI LOGIC		
Power (10^-11w)	Delay(s)	No. of Transistors	Power (10^-11w)	Delay (s)	No. of Transistors
4.43	6.78	66	2.69	2.59	22

The design for 16-bit CSLA is shown in fig 5.The schematic and simulated waveform of CSL A is shown in fig 6. During discharging process, the output energy which is stored can be recovered by moving backward the current source direction.

Energy dissipation is reduced in PMOS network and the energy stored in the output load capacitance, reused by reversing the current source direction in adiabatic switching technique. Table 4 shows the comparison of delay & power of logic functions in MOD-GDI and CMOS logic.A 16-bit CSLA was designed using CMOS logic and MOD-GDI logic, reduction in power-delay product in Mod-GDI logic can be achieved when compared to CMOS logic.In MOD-GDI logic, time delay is reduced and the number of transistors are also reduced.

V. CONCLUSION

A 16-bit CSLA adder was fabricated using CMOS technology and Mod-GDI technique. From the simulation results,45% reduction in power-delay product in Mod-GDI is observed. Mod-GDI approach performs a broad variety of logic functions by means of only two transistors.Mod-GDI gates lower the transistor count and the area required when compared to standard static CMOS and Domino CMOS based approaches. The problem of fabrication of GDI gates in standardnano-scale CMOS process is overcome by connecting the sources of PMOS and NMOS to VDD and GND respectively in Mod-GDI logic style. In short, the proposed Mod-GDI logic style based designs can be taken a better alternative in future.

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